

02-10-04

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February 9, 2004

VIA US MAIL

MAIL STOP DD
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: App No. 10/624,097; "Point to Point Memory Expansion Stacking System and Method"; Docket No. 0254-094-CIP-4/CIP-1

Dear Commissioner:

Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 143 references; and
4. a return postcard for confirmation of receipt.

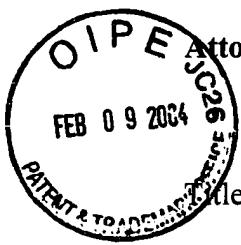
The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP


Pam Menke
Board Certified Legal Assistant in Civil Trial Law
Texas Board of Legal Specialization

/pm
enclosures



Attorney Docket No.: 0254-094-CIP-4/CIP1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Point to Point Memory Expansion System and Method

Application No.: 10/624,097

Filing Date: 07/21/2003

Inventor: James W. Cady, et al.

Assignee: Staktek Group, L.P.

Examiner: TBA

Group: 2818

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (nine sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

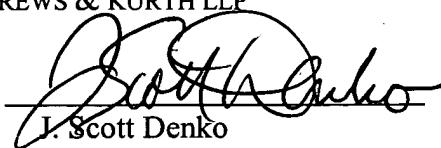
In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. A **duplicate copy of Form 1449 is enclosed.**

Respectfully submitted,

ANDREWS & KURTH LLP

By:



J. Scott Denko

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Feb. 9, 2004
Date

Form PTO-1449 (Modified)
(Rev. 11/92)U.S. Dept. of Commerce
Patent and Trademark OfficeINFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

(37 CFR 1.98(b))

FEB 09 2004
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PATENT & TRADEMARK OFFICE

ATTY. DOCKET NO. SERIAL NO.

0254-094-CIP-4/CIP-1 10/624,097

APPLICANT

Cady, et al

FILING DATE GROUP

7/21/03 2818

U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	4,763,188	8/9/1988	Johnson, Thomas	357/74		11/4/1987
	5,239,198	8/24/1993	Lin et al.	257/693		7/2/1992
	6,028,365	2/22/2000	Akram et al.	257/778		3/30/1998
	6,433,418	8/13/2002	Fujisawa et al.	257/696		4/29/1999
	6,208,521B1	3/27/2001	Nakatsuka, Yasuo	361/749		5/19/1998
	6,265,660B1	7/24/2001	Tandy, Patrick W.	174/52.4		8/18/2000

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	5-21697(A)	01/1993	Japan			Partial	
	57-31166(A)	02/19/1982	Japan			Partial	
	58-96756(A)	06/08/1983	Japan			Partial	
	58-112348(A)	07/04/1983	Japan			Partial	
	60-254762	12/1985	Japan	-	-	Partial	
	62-230027(A)	10/08/1987	Japan			Partial	
	63-153849(A)	06/27/1988	Japan			Partial	

OTHER DOCUMENTS
(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

Dense-Pac Microsystems, 16 Megabit High Speed CMOS SRAM DPS1MX16MKn3
Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5
Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993
Dense-Pac Microsystems, DPS512X16A3, Ceramic 512K X 16 CMOS SRAM Module
"Design Techniques for Ball Grid Arrays," William R. Newberry, Xynetix Design Systems, Inc.
"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.

EXAMINER

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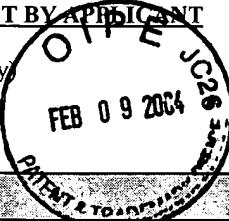
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				ATTY. DOCKET NO. 0254-094-CIP-4/CIP-1		SERIAL NO. 10/624,097	
(Use several sheets if necessary)				APPLICANT Cady, et al			
(37 CFR 1.98(b))				FILING DATE 7/21/03		GROUP 2818	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	6,300,679B1	10/9/2001	Mukerji et al.	257/738		6/1/1998	
	6,462,412B2	10/8/2002	Kamei et al	257/723		1/17/2001	
	6,465,893B1	10/15/2002	Khandros et al.	257/777		10/19/2000	
	6,486,544B1	11/26/2002	Hashimoto, Nobuaki	257/686		9/3/1999	
	6,560,117B2	5/6/2003	Moon, Ow Chee	361/749		8/30/2001	
	6,572,387B2	6/3/2003	Burns et al.	439/69		3/19/2002	
	6,590,282B1	7/8/2003	Wang et al.	257/686		4/12/2002	
	6,600,222B1	7/29/2003	Levardo, Melvin N.	257/686		7/17/2002	
FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	EP 461-639-A	12/1991	European			X	
	EP 0 298 211 A#	01/11/1989	European			X	
	EP 122-687-A	10/24/1984	European			X	
	SU 834-957	05/30/1981	Russian			Partial	
OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)							
	"Alterable Interposer Block for Personalizing Stacked Module Interconnections," <i>IBM Technical Disclosure Bulletin</i> , Vol. 30, No. 8, January 8, 1988, pp. 373-374.						
	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams						
	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division						
	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated						
	Teresa Technologies, Inc. – Semiconductor Intellectual Property, Chip Scale Packaging – Website pages (3)						
	"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.						
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APPLICANT	
Cady, et al	
FILING DATE	GROUP
7/21/03	2818

U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001
	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
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	US2002/0180022A1	12/5/2002	Emoto, Yoshiaki	257/686		7/19/2002
	6,072,233	6/6/2000	Corisis et al.	257/686		5/4/1998
	Re 36,916	10/17/2000	Moshayedi	257/723		04/22/1998
	3,436,604	04/01/1969	Hyltin	317/101		04/25/1966
	3,727,064	04/10/1973	Bottini	250/217		03/17/1971
	3,654,394	04/04/1972	Gordon	179/15 BL		07/08/1969
	3,746,934	07/17/1973	Stein	317/101		05/06/1971
	3,772,776	11/20/1973	Weisenburger	29/628		12/03/1969

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No

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(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)**

Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
"Vertically-Integrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

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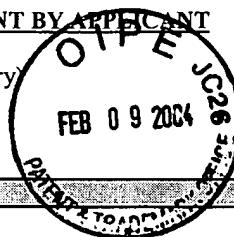
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				FILING DATE 7/21/03		GROUP 2818	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	4,103,318	07/25/1978	Schwede	361/388		05/06/1977	
	4,288,841	09/08/1981	Gogal	361/414		09/20/1979	
	4,398,235	08/09/1983	Lutz, et al	361/393		09/11/1980	
	4,406,508	09/27/1983	Sadigh-Behzadi	339/75		07/02/1981	
	4,437,235	03/20/1984	McIver	29/840		08/23/1982	
	4,513,368	04/23/1985	Houseman	364/200		05/22/1981	
	4,645,944	02/24/1987	Uya	307/243		09/04/1984	
FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
OTHER DOCUMENTS <i>(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)</i>							
	Chip Scale Review Online - An Independent Journal Dedicated to the Advancement of Chip-Scale Electronics. (Website 9 pages) Fjelstad, Joseph, Pacific Consultants L.L.C.						
	Flexible Thinking: Examining the Flexible Circuit Tapes. (Website 2 pages) Fjelstad, Joseph.						
	Die Products: Ideal IC Packaging for Demanding Applications - Advanced packaging that's no bigger than the die itself brings together high performance and high reliability with small size and low cost. (Website 3 pages with 2 figures) Larry Gilg and Chris Windsor. December 23, 2002.						
	Flexible Printed Circuit Technology - A Versatile Interconnection Option. (Website 2 pages) Fjelstad, Joseph. December 3, 2002.						
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				FILING DATE 7/21/03		GROUP 2818	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	4,696,525	09/29/1987	Coller, et al	439/69		12/13/1985	
	4,733,461	03/29/1988	Nakano	29/830		12/24/1985	
	4,821,007	04/11/1989	Fields, et al	333/238		02/06/1987	
	4,823,234	04/18/1989	Konishi, et al	361/386		07/01/1986	
	4,833,568	05/23/1989	Berhold	361/383		01/29/1988	
	4,862,249	08/29/1989	Carlson	357/80		04/17/1987	
	4,884,237	11/28/1989	Mueller, et al	365/63		03/17/1989	
	4,891,789	01/02/1990	Quattrini, et al	365/63		03/03/1988	
	4,911,643	03/27/1990	Perry, et al	439/67		08/03/1989	
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION							
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7/21/03 GROUP 2818

U.S. PATENT DOCUMENTS

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	5,041,015	08/20/1991	Travis	439/492		03/30/1990
	5,099,393	03/24/1992	Bentlage, et al	361/413		03/25/1991
	5,104,820	04/14/1992	Go, deceased, et al	437/51		06/24/1991
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	5,198,888	03/30/1993	Sugano, et al	257/686		12/20/1990
	5,222,014	06/22/1993	Lin	361/414		03/02/1992
	5,224,023	06/29/1993	Smith, et al.	361/412		02/10/1992
	5,241,454	08/31/1993	Armeen, et al	361/744		01/22/1992
	5,247,423	09/21/1993	Lin, et al	361/719		05/26/1992
	5,259,770	11/09/1993	Bates, et al	439/66		03/19/1992
	5,261,068	11/09/1993	Gaskins, et al.	395/425		05/25/1990
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	5,279,029	01/18/1994	Burns	29/856		05/11/1993
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	5,289,062	02/22/1994	Wyland	307/577		03/23/1993
	5,311,401	05/10/1994	Gates, Jr. et al	361/760		07/09/1991
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

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OTHER DOCUMENTS

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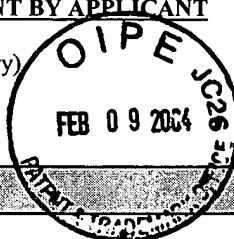
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				APPLICANT Cady, et al			
				FILING DATE 7/21/03		GROUP 2818	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	5,343,075	08/30/1994	Nishino	257/686		06/22/1992	
	5,347,428	09/13/1994	Carson, et al	361/760		12/03/1992	
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	5,420,751	05/30/1995	Burns	361/707		10/08/1993	
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	5,484,959	01/16/1996	Burns	174/524		12/11/1992	
	5,493,476	02/20/1996	Burns	361/735		05/22/1995	
	5,499,160	03/12/1996	Burns	361/704		01/30/1995	
	5,514,907	05/07/1996	Moshayedi	257/723		03/21/1995	
	5,523,619	06/04/1996	McAllister, et al	257/686		11/03/1993	
	5,541,812	07/30/1996	Burns	361/735		09/11/1995	
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	5,543,664	08/06/1996	Burns	257/787		01/20/1995
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	5,631,193	05/20/1997	Burns	29/827		06/30/1995
	5,644,161	07/01/1997	Burns	257/668		06/07/1995
	5,654,877	08/05/1997	Burns	361/713		08/18/1995
	5,776,797	07/07/1998	Nicewarner, Jr., et al	438/107		07/02/1997
	5,801,437	09/01/1998	Burns	257/685		08/11/1995
	5,805,422	09/08/1998	Otake, et al	361/749		08/15/1997
	5,835,988	11/10/1998	Ishii	257/684		10/24/1996
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	5,926,369	07/20/1999	Ingraham, et al	361/699		01/22/1998
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						Yes	No

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	5,953,215	09/14/1999	Karabatsos	361/767		06/26/1998	
	6,014,316	01/11/2000	Eide	361/735		06/10/1998	
	6,028,352	02/22/2000	Eide	257/686		06/10/1998	
	6,172,874B1	01/09/2001	Bartilson	361/719		04/06/1998	
	6,266,252B1	07/24/2001	Karabatsos	361/788		09/13/1999	
	6,233,650B1	05/15/2001	Johnson et al.	711/5		04/01/1998	
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